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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,550	04/18/2001	Boris A. Babaian	020181005100	9262
20350	7590	11/19/2004	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834				HOGAN, MARY C
ART UNIT		PAPER NUMBER		
		2123		

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/838,550	BABAIAN ET AL.
	Examiner	Art Unit
	Mary C Hogan	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 31 December 2001.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-34 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 31 December 2001 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 8/9/01.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

1. This application has been examined.
2. **Claims 1-34** have been examined and rejected.

Specification

3. The disclosure is objected to because of the following informalities. Appropriate correction is required.
4. **Page 1, lines 15-20** contain references to application numbers that have not yet been added.

Drawings

5. The drawings are objected to because of the following: **Figure 2**: Physical Memory 108 is cut off and appears to be misspelled. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. **Claims 7 and 14** are objected to because of the following informalities. Appropriate correction is required.
7. **Claim 7** is missing a period at the end of the sentence.
8. **Claim 14** recites “operating foreign system code”, making the claim unclear in meaning.

Claim Interpretation

9. **Claim 14** recites “operating foreign system code”, making the claim unclear in meaning. The claim was interpreted to read “foreign operating system code”.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. **Claims 1-34** are rejected under 35 U.S.C. 102(b) as being anticipated by **Ryba** et al (U.S. Patent Number 5,574,936), herein referred to as **Ryba**.

12. As to **Claims 1, 10,13,18,22 and 28**, **Ryba** teaches: a method for translating foreign binary code for execution on a host computer system where the host computer system is architecturally distinct from the foreign architecture, said host computer system providing a foreign and a host virtual space, said method comprising the steps of

a physical memory (Figure 1, element 8)

configuring a first and second virtual space (column 6, lines 50-55 “Pages”);

storing foreign code in said first virtual space (column 4, lines 27-31);

storing a plurality of translation processes in said second virtual space (column 6, lines 56-58-63);

storing binary translated code in said second virtual space, said binary translated code

comprising at least a portion of said foreign code in said first virtual space (column 6, lines 17-21, column 7, lines 1-5);

executing said binary translated code (column 5, lines 30-32);

detecting a memory access that attempts to modify a memory location (column 8, lines 61-

64,column 14, line 6-19);

determining the status of the accessed memory location (column 14, lines 9-19);

if the status permits access, modifying the memory location (column 14, lines 16-19);

if the status does not permit access, generating a page fault exception (column 14, lines 15-16).

defining a first page table to map said foreign code from said first virtual space to physical memory (column 6, lines 10-16);

defining a second page table to map said binary translated code to said second virtual space (column 6, lines 17-21);

associating information relating to said foreign code with said page table, said information determining if a portion of said foreign code and data in said virtual space may be accessed (column 6, lines 50-55, column 2, lines 46-56).

means for maintaining said first and second page tables in response to changes generated by executing said binary translated code (column 2, lines 45-65)

providing a support software layer, said software layer functioning as an operating system for controlling the binary translation of said foreign code and data and for detecting a write access to physical memory of said host computer system, said physical memory corresponding to said foreign virtual space by said host code (column 4, lines 11-18, column 9, lines 47-55, column 10, lines 25-30).

an emulated supervisor flag associated with portions of said host binary code where said support software layer accesses said supervisor flag prior to executing a write access into said foreign and host virtual spaces (column 10, lines 4-5).

13. As to **Claim 2, Ryba** teaches: the system of claim 1 wherein said maintaining means further comprises a register dedicated to track code modification to maintain correspondence between foreign and binary translated host code flag, associated with each page of memory, to indicate modification of said page of memory (column 6, line 66-column 7, line 5).

14. As to **Claim 3, Ryba** teaches: the system of claim 1 further comprising a flag, associated with each page of memory, to indicate a change in a page in foreign virtual space (column 2, lines 46-48).

15. As to **Claim 4, Ryba** teaches: the system of claim 1 further comprising means for restricting access to a page of memory in foreign virtual space (column 14, lines 6-16).

16. As to **Claim 5, Ryba** teaches: the system of claim 4 wherein said restricting means comprises means for generating a trap (column 3, lines 3-14 “protection exception”).

17. As to **Claim 6, Ryba** teaches: the system of claim 1 wherein said first page table maps foreign code to a portion of physical memory (column 5, lines 44-46, column 6, lines 53-55).

18. As to **Claim 7, Ryba** teaches: the system of claim 6 wherein said first page table includes a first and second bit associated with each page of memory in foreign virtual space, said first bit indicating whether a page of memory in foreign virtual space is write protected and said second bit indicating a locked page of memory (column 1, line 44-59, column 2, lines 5-7, lines 46-50).

19. As to **Claim 8, Ryba** teaches: the system of claim 7 further comprising means for determining the state of said first bit and invoking a page fault exception upon a change in page contents (column 14, lines 6-16).

20. As to **Claim 9, Ryba** teaches: the system of claim 1 wherein said first page table includes a first and second bit associated with each page of host memory, said first bit indicating whether access to said page is restricted (column 2, line 47); said second bit indicated whether access to said page in said foreign virtual space is accessible only in a supervisor mode of operation (column 2, line 63 wherein there is a bit to indicate supervisor state).
21. As to **Claim 11, Ryba** teaches: the method of claim 10 further comprising the step of if the status indicates access is limited to code executing in an emulated target supervisor mode, determining if the computer system is executing in an emulated target supervisor mode (column 10, lines 4-5); and if the status indicates that the code is not executing in said emulated target supervisor mode, generating an exception (column 14, lines 6-7, lines 12-16).
22. As to **Claim 12, Ryba** teaches: the method of claim 11 further comprising the steps if access is allowed, checking the address against a range of addresses; and determining if the memory location to be accessed is currently in memory (column 4, lines 28-33, column 14, lines 16-19).
23. As to **Claim 14, Ryba** teaches the method of claim 13 further comprising the step of using said information to determine if said foreign code comprises operating foreign system code (column 2, lines 46-56, line 63, column 6, lines 23-29, 50-55).
24. As to **Claim 15, Ryba** teaches: the method of claim 14 further comprising the step of using said information to detect modification of said code and data in said foreign virtual space (column 3, lines 3-14).
25. As to **Claim 16, Ryba** teaches: the method of claim 15 further comprising the step of invoking a binary translation process upon detection of modification of said code and data in said foreign virtual space to generate binary translated code corresponding to said code and data in said foreign virtual space (column 13, lines 25-41).
26. As to **Claim 17, Ryba** teaches: the method of claim 13 further comprising the step of using said first page table to map a logical address of said foreign code to a compatibility region of physical memory in said host computer system (column 6, lines 53-55).
27. As to **Claim 19, Ryba** teaches: the method of claim 18 further comprising the step of executing said support software layer in said second virtual memory, said support software layer adapted to managing I/O operations (column 10, lines 45-49).
28. As to **Claim 20, Ryba** teaches: the method of claim 19, further comprising the step of virtualizing a restricted set of functions (column 5, lines 13-16).

29. As to **Claim 21**, **Ryba** teaches: the system of claim 20, further comprising the step of virtualizing peripheral components expected in a target operating system (column 4, lines 19-24 “devices and other resources”).

30. As to **Claim 23**, **Ryba** teaches: the system of claim 22 wherein said support software layer comprises means for performing binary translation of said foreign code and said host code (column 6, lines 17-21).

31. As to **Claim 24**, **Ryba** teaches: the system of claim 23 further comprising an access watch engine adapted to detect a write access to physical memory in said host computer system (column 14, lines 6-16).

32. As to **Claim 25**, **Ryba** teaches: the system of claim 22 further comprising means for detecting write accesses to physical memory corresponding to said foreign virtual space (column 14, lines 6-16).

33. As to **Claim 26**, **Ryba** teaches: the system of claim 25 further comprising means for detecting write accesses to physical memory corresponding to memory mapped peripherals (column 14, lines 6-16).

34. As to **Claim 27**, **Ryba** teaches: the system of claim 25 further comprising means for virtualizing a restricted set of available hardware to produce enough resources to run resource-consuming firmware (column 5, lines 9-24).

35. As to **Claim 29**, **Ryba** teaches: the system of claim 28 further comprising means for detecting said supervisor flag and marking selected portions of said foreign and host virtual spaces as accessible only in an emulated supervisor mode, said detecting means coupled to said support software layer (column 2, lines 46-65, column 6, lines 6-7).

36. As to **Claim 30**, **Ryba** teaches: the system of claim 28 further comprising a page lock flag, said page lock flag indicating restricted access to selected portions of said foreign virtual space (column 2, lines 46-48).

37. As to **Claim 31**, **Ryba** teaches: the system of claim 30 further comprising means for detecting the state of said page lock flag (column 14, lines 7-12).

38. As to **Claim 32**, **Ryba** teaches: the system of claim 28 further comprising a common structure supported in hardware for maintaining said the foreign and host virtual spaces (Figure 1, element 8).

39. As to **Claim 33**, **Ryba** teaches: the system of claim 28 further comprising an access watch engine for detecting write accesses to said physical memory (column 14, lines 4-7).

40. As to **Claim 34**, **Ryba** teaches: The system of claim 28 further comprising an emulated target supervisor flag for initiating binary translation from said foreign binary code to said host binary code (column 9, line 66-column 10, line 5).

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Conclusion

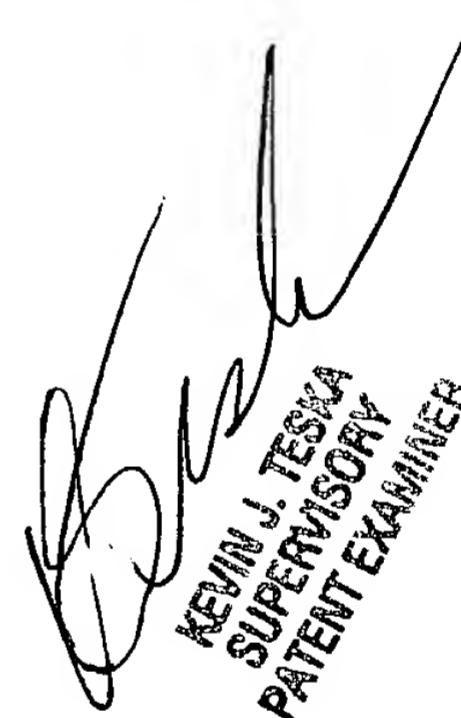
41. The prior art made of record, see PTO 892, and not relied upon is considered pertinent to applicant's disclosure, careful consideration must be given prior to Applicant's response to this Office Action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 571-272-3712. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C Hogan

Examiner

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KEVIN J. TESKA
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